Insulating Biomaterials
N01-NS-9-2323

Third Quarterly Progress Report
April-June, 2000

Neural Prosthesis Program
National Institutes of Health
National Institute of Neurological
Disorders and Stroke

InnerSea Technology

Contributors:
David J. Edell, PI
Lydia Y. Li, Surgery and Testing
Ying Ping Liu, Assembly and Testing
Sean Sexton, Instrumentation and Software
Karen K. Gleason, Chem Eng (MIT)
Thomas B. Casserly, Grad Student, Chem Eng (MIT-HFCVD Silicones)
Shashi K. Murthy, Grad Student, Chem Eng (MIT-CVD Fluoro-silicones)

Instrumentation for In-Vitro Monitoring of Long Term Devices

Data from the 384 channel electrometer system has been difficult to interpret in the last attempt at a detailed review. Apparently there is an intermittent software or hardware error that is corrupting data. A thorough examination of the system has begun in an effort to determine the problem(s) and hopefully understand it well enough to either re-construct the data or at least eliminate the corrupted data.

Silicon Corrosion

In order to determine the uptake of biochemicals into silicones implanted in biological systems, 3 rabbits were implanted with a total of 9 strips of MED4-4220 silicone from Nusil. Each strip was 2x8cm and approximately 1mm thick. These silicone samples will be left in place for 6 months, then one sample from each rabbit will be removed and sent to an analytical laboratory for analysis of the absorbed materials. From this information it may be possible to create chemical specific soak environments to accelerate the effects of particular biochemicals on silicones.

Another issue for implanted silicon devices is the possible corrosion of silicon in the biological environment. Corrosion was incidentally observed in a previous experimental attempt to qualify the uptake of biochemicals by silicones. In that experiment, silicon samples used as supports for silicones in an FTIR analysis were severely corroded after 1 year implantation. A subsequent experiment where University of Michigan neural probes were implanted for 1 year showed no evidence of corrosion. The samples that corroded were N-type while those that did not were P^{++}.

In order to determine the corrosion characteristics of silicon, an experiment was designed with the help of Jamie Hetke of the National Center for Neural Communication Technology (CNCT) at the University of Michigan to determine the necessary characteristics of silicon for corrosion resistance. Three types of

silicon were embedded in silicone carriers and implanted into the same three animals used for soaking the blank silicone pieces. The three types of silicon chosen were relevant to implantable silicon devices fabricated by the CNCT and elsewhere: 1) P-type starting silicon for passive probes; 2) N-type silicon; 3) P-type silicon patterned with the P^{++} boron etch stop diffusion used for passive probes. The n-type silicon was included to confirm the previous observations. Implants patterned with normal deep diffusions may illustrate differential etching of the lightly doped p-substrate while the highly doped P^{++} region remains untouched. The lightly doped P silicon may indicate whether it is the type of dopant or the dopant concentration that is important.

Three blank silicone strips and three silicon carrying silicone strips were placed in subcutaneous pockets parallel to the ribs over the animal's back. Surgeries were uneventful and the animals recovered well. The first animal will be sacrificed in November to harvest the devices and to begin evaluations.

Mechanical Properties of Silicone

It has been observed in previous work that silicones can undergo substantial mechanical alterations during saline soak and animal implantation. Previously, simple rods of silicone were implanted in rabbits and were subsequently retrieved for mechanical testing. Several silicones underwent substantial changes in Young's Modulus after 6 months implantation. A more controlled experiment with uniform rings of silicone was begun. Two rabbits were implanted with 6 rings of silicone. Prior to implantation, Young's Modulus on each ring was measured. After 6 months (January, 2000), 2 rings from each animal will be removed and re-tested. Additional samples will be removed at intervals indicated by the in-vitro testing.

Passivation Chip

PassChip die were assembled into an implantable structure complete with Tadiran lithium batteries and output LED. However, these devices were non-

functional. Eventually the assembly failures were traced back to chip failure. Inspection of the wire bonder revealed a broken ground wire on the hot stage, and corroded grounding connections to several other points on the bonder. In addition, the humidity was low which could have contributed to damage of the chip by static discharge. The temporary cleanroom where these devices were assembled also had no air ionization at the time. The wire bonder stage was rebuilt to provide more reliable ground protection, and more reliable heating of the devices as well. The corroded ground connections were repaired and particular attention was given to the ground return for the electronic flame-off. The electronic flame-off provides a high voltage spark to the end of the bond wire that hangs below the capillary after the second bond is made for a wire bond connection which may have caused excessive charge buildup on the chip with the poor grounding.

An air ionizer was installed to minimize static charge buildup on surfaces. Then a new bonding sequence was devised in which the large lead wires from the substrate used to assemble the circuit were connected together with small jumper wires and grounded prior to making the first bond. The first bond made is then to the substrate and chip shield connections. The second is to the power supply connection. At this point, the circuit is fairly well protected. Even the exposed external device bonding pads, and the external IDE and external large area pad are surrounded by grounded silicon or metal at this stage. After the bonds are completed, and the external leadwires are attached to the power supply or connector (with shorting bar in place), the small jumper wires were removed to allow operation of the circuit.

A battery supply was constructed which consisted of two glass sealed Tadiran lithium batteries connected in series to provide 7.3 volts, a voltage regulation circuit to set the voltage to 5.0 volts, and a 10K limiting resistor with 0.1uF filter capacitor. The components were cleaned in flux remover (freon and isopropyl alcohol) followed by an isopropyl alcohol rinse. After drying, the power unit was embedded in silicone and attached to the circuit. This circuit was functional.

A system diagram is shown in Figure 1. Charge from leakage current (I_{leak}) is integrated onto C_i of the input integrator continually. When the output of the on-chip integrator drops below Vref, C_i is reset to the "high" Schmitt trigger threshold by a high impedance switch. The output of the integrator is monitored by a readout capacitor which periodically samples the integrator output voltage onto a readout capacitor. The resulting charge packet is then removed by the readout current source I_o or I_m in the case of the marker channel. When the output capacitor voltage drops below Vref, the output Schmitt trigger turns on the output LED and resets the output capacitor voltage to the next voltage level to be transmitted. The time it takes to remove the charge from the readout capacitor is proportional to the on-chip integrator voltage. The decoder receives the light pulse and converts it to a voltage pulse which is used to reset the decoder integrator. The voltage that the decoder integrator attains prior to reset is proportional to the time between incoming light pulses and hence is proportional to the on-chip integrator voltage being transmitted.

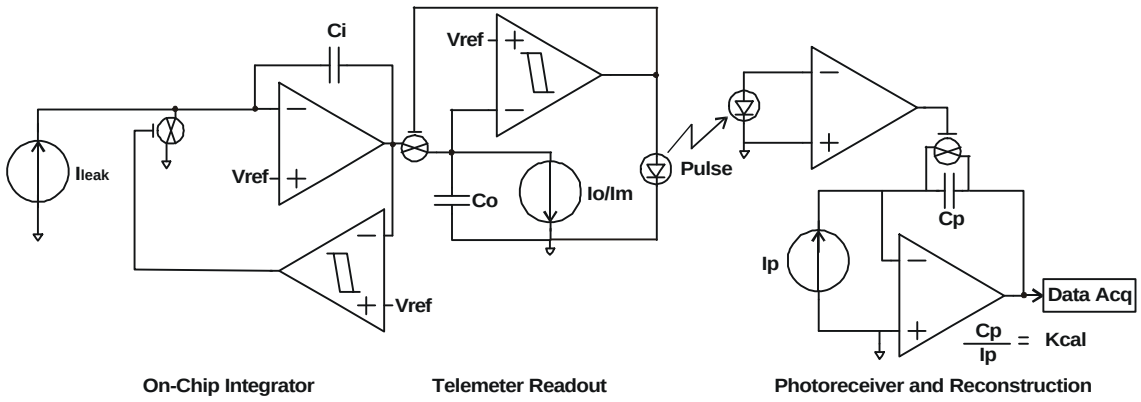


Figure 1: Functional diagram of PassChip system.

A reconstructed on-chip integrator output is shown in Figure 2. This output waveform was from an integrator connected to a fairly high leakage current test device, a 3600μm^2 PN diode. The non-linearity of the chip integrator output is apparent in the first part of the integrator response following reset. This is caused by use of an n-well capacitor for the integration capacitor. Originally, this

capacitor was chosen since the gate oxide is the lowest leakage oxide in the

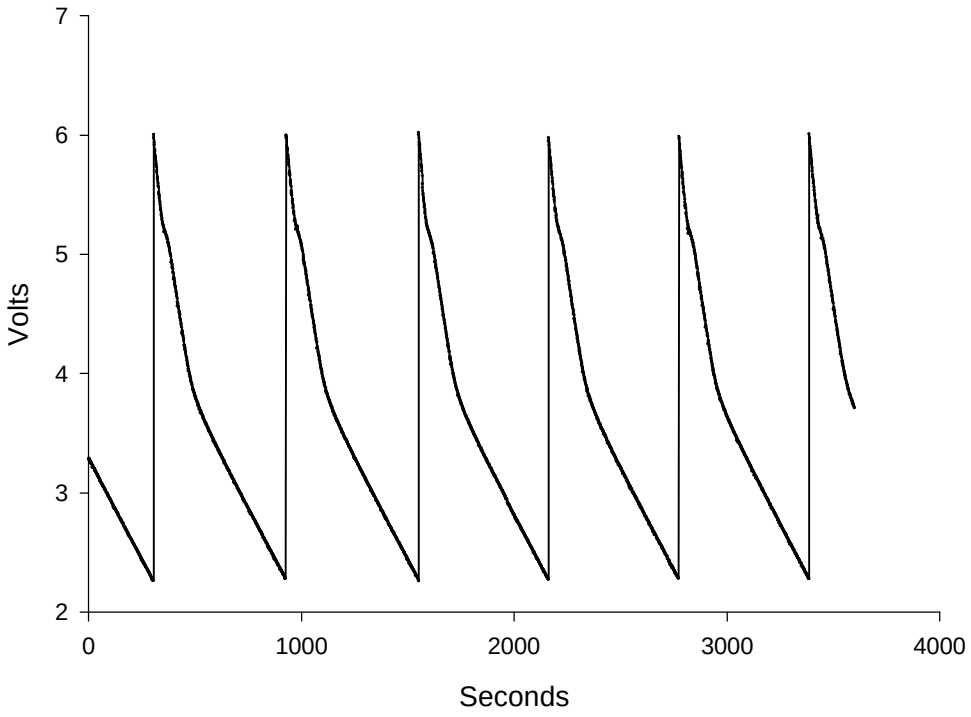


Figure 2: Reconstructed output of on-chip integrator output for large area diode test device.

integrated circuit. However, as the bias on the capacitor changes, this PMOS capacitor changes from an inverted state (just after reset) to a depleted state and finally to an “off” state. These different operating points change the capacitance of the integrator, which changes the slope of the integrator output. Since the inversion layer of this MOS capacitor is not electrically connected, the capacitor characteristic appears primarily as the series connection of the depletion layer and the oxide capacitance. Thus with full bias across the capacitor, the capacitance is at a minimum due to the series connection and the slope is at maximum. As the voltage decreases during the integration process, the depletion thickness decreases causing an increase in the capacitance. If the change is very slow, the inversion layer is also involved in this capacitance, which tends to short out the depletion capacitance. The magnitude of this effect depends on the rate of change of the gate-substrate voltage and the lifetime of the minority carriers in the n-well. These factors make it very difficult to reconstruct the actual input leakage current. However, the final 1volt or so of the

integrator output characteristic is quite linear and represents the capacitance of the gate oxide alone. When the integrator output voltage drops below 2.4 volts, the on-chip integrator resets by connecting the integration node to zero volts through a 1nA current source buffered by a high impedance p-channel switch. The choice of the p-channel switch was made to ensure that any leakage from the switch would be a positive current so integrators would always reset, even if there were no leakage current. Use of the active integrator circuitry ensures that the bias across the device under test is constant, and equal to the power supply minus the reference potential of 2.4 volts. With a 7.4 volt power supply (provided by 2 thionyl chloride-lithium batteries), the devices under test will be biased continually at 5 volts.

An example of the output pulse train and decoder integrator output is shown in Figure 3. The wide pulse interval is the marker channel. The subsequent intervals are channels 1-14. Signal reconstruction occurs by sampling and holding the decoder integrator voltage at the time of the decoder integrator reset caused by the arrival of the interval ending pulse.

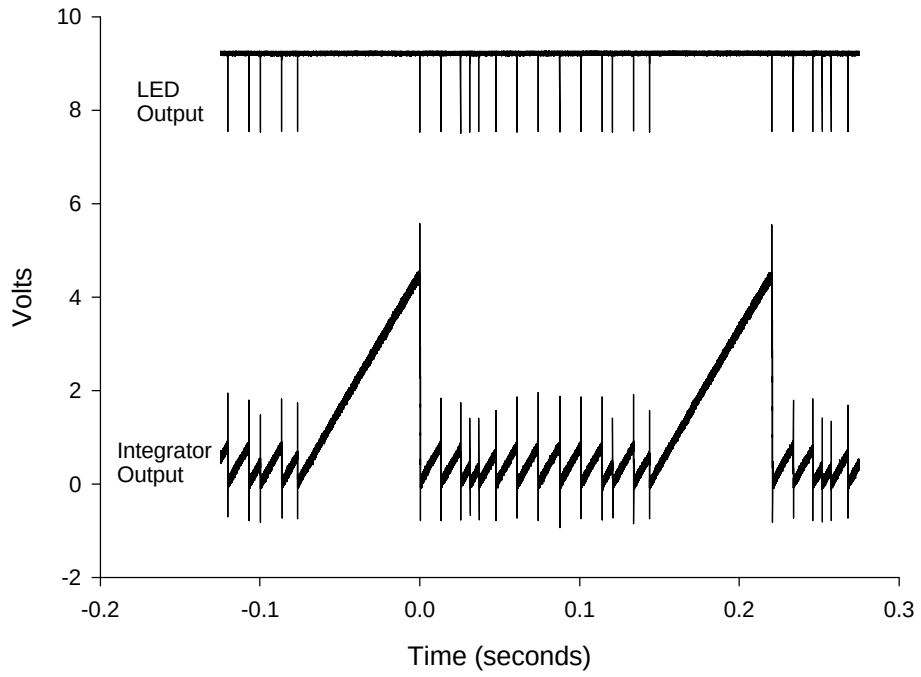


Figure 3: Output pulse train from PassChip (LED OUTPUT) and decoder integrator output.

Calibration is accomplished by knowing the on-chip integrator capacitance, the encoder capacitance, encoder integration current, and decoder integration current and capacitance. Design calibration was based on the repeatability of the MOSIS gate capacitors. Typcially there is much less than 10% error in the MOSIS calibration. The bias current used to set the current of the readout integrator was directly measured. This allows computation of the overall transfer capacitance as shown in Equation 1.

$$C_{eff} \cong \frac{C_i I_o K_d}{C_o}$$

where:
C_{eff} = *Effective system capacitance (2.49pF)*
C_i = *Chip integrator capacitance (2.5pF)*
I_o = *Chip telemeter readout current (17.4nA)*
K_d = *Decoder "transtimeance" (2.06mSec/Volt)*
C_o = *Chip telemeter readout capacitance (36pF)*

Equation 1: Computation of effective capacitance for signal encoding/decoding process.

The device leakage current can then be computed from the slope of the decoder output waveform according to Equation 2.

$$I_l \cong C_{eff} \times \partial V / \partial t$$

Equation 2: Computation of leakage current from effective capacitance and derivative of the decoder output voltage.

Operation of the pass chips at 7.4 volts is not possible. When these chips were operated at 7.4 volts, resetting of the shift register was erratic. There is no obvious reason why this behavior should occur. However, the MOSIS process used to fabricate these devices was limited to a supply voltage of 5 volts according to process specifications. Thus it's possible to imagine that hot electron injection or some other phenomenon is responsible for the erratic behavior.

Results of initial testing of one pass chip operated at 6 volts are summarized in Table 1. Currents appear to be reasonable for an integrated circuit structure. The open circuit integrator (channel 14) shows the minimum current that can be expected with the reset switch leakage current probably accounting for all of the observed current. These reading were relatively noisy (standard deviation on the order of 1/3 of the measured current. There was excess noise from the photodectector pickup as well as the decoder.

Channel	Device	Volts or Amperes	Std.Dev.
1	Battery Volts (5.915) from Marker	5.918	0.015
2	M1 IDEA w/M2Shield	1.40E-14	6.25E-15
3	M1 M2 Waffle w/Poly+M2 Shield	9.82E-15	5.09E-15
4	Diode near M2 shield edge	8.83E-14	2.63E-14
5	Diode	9.34E-14	2.93E-14
6	Gate on N-well Waffle	2.24E-14	1.51E-14
7	M2 IDEA bare on surface	8.04E-15	3.75E-15
8	P2 IDEA w/M2 shield	8.43E-15	6.24E-15
9	P1 IDEA w/M2 shield	7.82E-15	3.27E-15
10	P1-P2 Waffle w/M2 shield	1.24E-14	8.03E-15
11	M2-out Large Pad	5.57E-15	2.49E-15
12	External Device	nc	nc
13	M1-P2 w/M2 shield	6.21E-15	4.01E-15
14	Open Circuit Integrator	9.87E-15	3.74E-15

Table 1: Example results from packaged PassChip using design calibration numbers.

The pickup and decoder required further optimization to minimize noise and to maximize sensitivity. These efforts are in progress. The decoder board mixes analog and digital circuitry, and must handle high speed pulse edges in order to accurately measure the time between pulses. The photodetector must transduce the photo signal to an electrical signal, and then detect the leading edge of the photopulse accurately. This also requires high speed analog circuitry to optimize the measurement of the time interval between leading edges of the light pulses. These efforts will be completed next quarter.

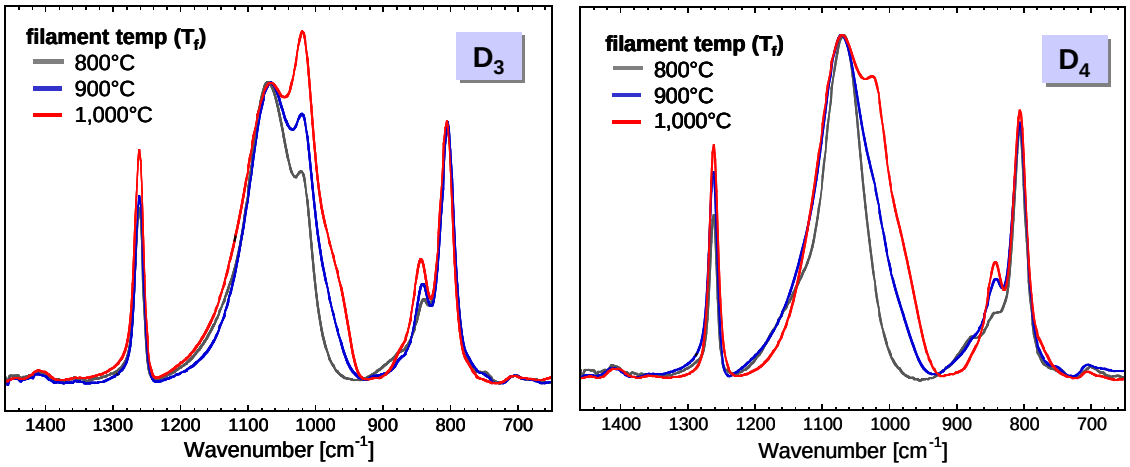
Interdigitated Electrode Arrays for Evaluation of Intra-Cortical Insulators

Intra-cortical Interdigitated Electrode Arrays (IDEs) were designed in collaboration with Jamie Hetke of the National Center for Neural Communication Technology at the University of Michigan. These arrays will be used to test

deposited films for long term surface insulation resistance when chronically implanted in the cortex of animals. Four IDEs will be located in a column at 200μm intervals along one of the center shafts with the closest approximately 500μm away from the tip. These will be used to check for local surface conductivity, local variations along the shaft, and far reaching surface conductive pathways along the shaft separated by 200μm, 400μm, or 600μm (by pairing half of 2 IDEs). Three additional IDEs will be located adjacent to a central IDE to form a row of 4 (with one on each shaft) approximately 700μm away from the tips. This row will be used to check for variations in local surface conductivity due to shaft location during coating (in a plasma for instance), and to quantify bulk material characteristics independent of surface leakage properties. Since there were 2 bonding pins leftover, an IDE was located at the tip of one shaft to allow evaluation of shaft tip effects. 3μm traces and spaces were used to form the IDEs in iridium. During the next quarter the design details will be implemented by Ms. Hetke and refined before the next run of custom devices.

CVD Silicone

The chemical structure of HFCVD films was evaluated by Fourier transform infrared spectroscopy (FTIR). Consistent trends were observed as a function of filament temperature for both precursors, D3 and D4. **Figure 4** A and B show the siloxane stretch regions of the FTIR spectra for the filament temperatures. Note that the intensity of the right side of the doublet can be systematically varied. Further work is need to access the chemical significance of this shoulder and whether this will have an impact on the properties required for biopassivation coatings such as dielectric constant, flexibility, and adhesion.



A **B**

Figure 4: The siloxane stretch region of the FTIR region for HFCVD silicone films at three different filament temperatures. Plot (A) shows the right hand shoulder is always present in the films deposited from D3. However, the intensity of the shoulder increases with increasing filament temperature. Plot (B) shows the shoulder is absent in the film deposited from D4 at low filament temperature, but appears at the higher temperature.

Fluorocarbon /Silicone Copolymers:

A new approach to making these materials was investigated. Two monomer species were used: hexafluoropropylene oxide (HFPO) and hexamethylcyclotrisiloxane (D_3). This choice was motivated by the fact that they

are relatively simple molecules and have been shown to be effective precursors individually. The technique used was HFCVD with a tantalum filament. The FTIR of one of the deposited films (Figure 5) suggests that a copolymer film has been successfully deposited.

Reproducing this result has proved difficult as there appear to be some materials compatibility issues in the CVD reactor. To deposit the copolymer, filament temperatures of about 700 C are required. This is higher than the temperature range required for the pure fluorocarbon films (400-600 C). The higher temperature results in more fluorine activity in the gas phase and some of the ceramic parts in the reactor failed. Redesign to eliminate these components has begun.

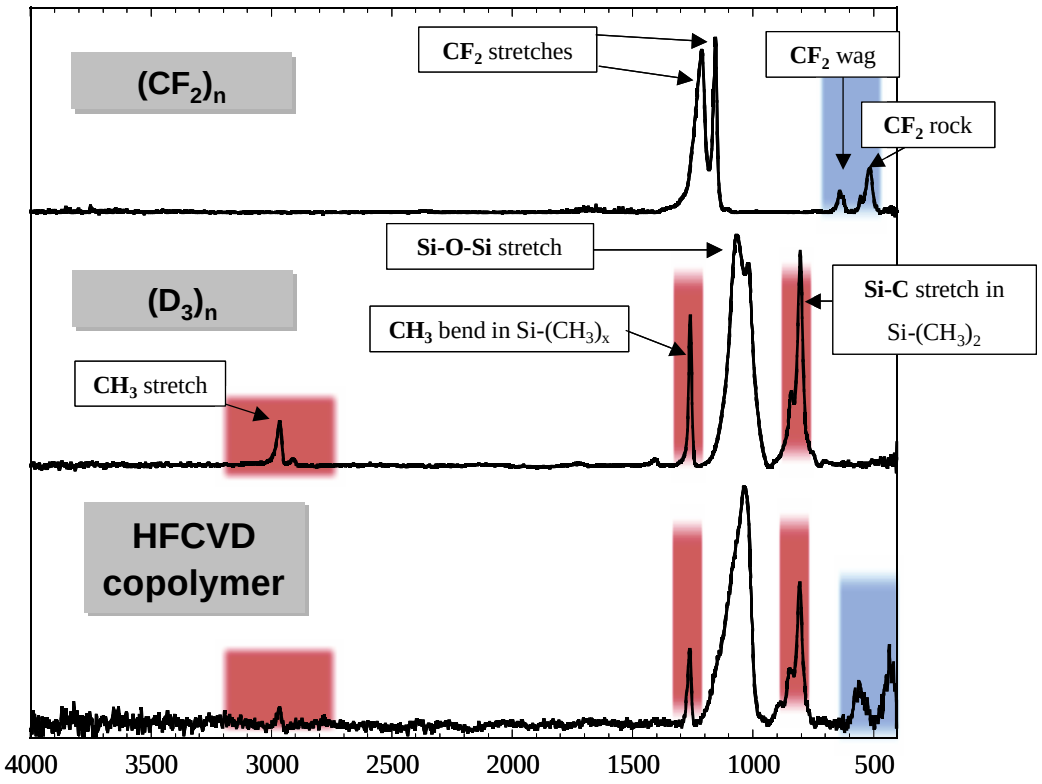


Figure 5: Comparison of the FTIR spectra for fluorocarbon/silicon copolymer film grown by HFCVD from HFPO and D3 (bottom), an HFCVD fluorocarbon film (top), and a HFCVD silicone film (middle).